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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/878,556	06/11/2001	S. Sundar Kumar Iyer	FIS9-2000-0372-US1	3210

7590 08/14/2002  
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EXAMINER

CHEN, JACK S J

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 08/14/2002

3

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.  
09/878,556

Applicant(s)  
Iyer et al.

Examiner  
Jack Chen

Art Unit  
2813



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Jun 11, 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-2 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15-18 is/are allowed.
- 6) ☒ Claim(s) 1, 6-8, 11-14, 19-21 is/are rejected.
- 7) ☒ Claim(s) 2-5, 9-10 is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some\* c) ☐ None of:

- ☐ Certified copies of the priority documents have been received.
- ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
- ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\*See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2 6) ☐ Other:

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### **DETAILED ACTION**

1. In response to the communications dated June 11, 2001, claims 1-21 are active in this application.

#### ***Information Disclosure Statement***

2. The information disclosure statement filed June 11, 2001 has been considered.

#### ***Oath/Declaration***

3. Oath/Declaration filed on June 11, 2001 has been considered.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -  
(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

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5. Claims 1, 6-8, 13-14, 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Cho, U.S./6,143,669.

Cho discloses a method for forming oxide layers of varying thickness across a semiconductor substrate surface, which comprises patterning and blocking a semiconductor substrate surface 20 with a layer of photoresist material PR2 (fig. 2B); removing a portion of the photoresist material layer to expose a device isolated region on a blocked semiconductor substrate surface (fig. 2B); increasing a differential oxidation rate value of an exposed semiconductor substrate surface (figs. 2C-2D, this is done by implanting Ge ions); removing the layer of photoresist material (fig. 2D); oxidizing the semiconductor substrate surface (fig. 2F); forming a first oxide layer 24a having a first thickness on the exposed semiconductor substrate surface; and forming a second oxide layer 24b having a second thickness on the blocked semiconductor substrate surface, wherein the first thickness is greater than the second thickness (fig. 2F), see figs. 2A-2F and related text in cols. 1-6.

Regarding claim 6, Cho further shows forming a shallow trench using shallow trench isolation (col. 2, lines 60-65).

Regarding claim 7, Cho inherently shows filling the shallow trench to form a device isolation region since it is the trench isolation (col. 2, lines 60-65).

Regarding claim 8, Cho further shows removing the portion of the photoresist layer further comprises etching the photoresist (col. 3, lines 1-10).

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Regarding claim 13, Cho further shows forming the first oxide layer having the first thickness on the exposed semiconductor substrate by growing the first oxide layer (col. 3, lines 56-66).

Regarding claim 14, Cho further shows forming the second oxide layer having the second thickness on the block semiconductor substrate surface by growing the second oxide layer (col. 3, lines 56-66).

Regarding claim 19, Cho discloses a method for forming oxide layers of varying thicknesses across a semiconductor substrate surface, which comprises photomasking a semiconductor substrate 20 surface with a photoresist material PR2 (fig. 2B); etching a portion of the semiconductor substrate surface (fig. 2C); increasing a differential oxidation rate value of an etched portion of the semiconductor substrate surface (fig. 2D, this is done by implanting Ge ions); stripping the photoresist material (fig. 2D); oxidizing the semiconductor substrate surface (fig. 2F); and growing two or more oxide layers 24a/24b, wherein a first oxide layer 24a has a thickness greater than a second oxide layer 24b thickness (fig. 2F).

Regarding claim 20, Cho further shows forming the first oxide layer on the etched portion of the semiconductor substrate surface (fig. 2F).

Regarding claim 21, Cho further shows forming a second oxide layer on a non-etched portion of the semiconductor substrate surface (fig. 2F).

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***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho, U.S./6,143,669.

Cho disclosed above, and in particular, Cho shows *forming* (not limited to oxidation method and other methods) the first and second oxide layers on the substrate; however, Cho does not explicitly show forming the first and second oxide layers on the substrate by depositing method. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Cho by depositing the oxide layers instead of using oxidation method since both of the methods are well known as the alternate methods for forming the oxide layers.

***Allowable Subject Matter***

8. Claims 2-5, 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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9. Claims 15-18 are allowable over the prior art of record.

10. The following is an examiner's statement of reasons for allowance: The prior art of record neither teach nor make it obvious the claimed limitation of the instant application as *a whole* as recited in claims 15. In particular, the prior art does not teach or suggest (in addition to other elements/processes in the claim) etching a portion of the semiconductor substrate surface and converting a non-porous semiconductor substrate material into a porous semiconductor substrate material.

### *Conclusion*

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hasegawa, U.S./6,091,109; Inaba, U.S./6,300,197 B1 and Crowder et al., U.S./6,335,262 B1 also disclose the similar methods for forming the thin and thick oxide layers.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (703) 308-5838. The examiner can normally be reached on Monday-Friday (alternate Monday off) from 8:30 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703)306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

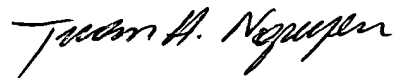
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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.



Jack Chen

August 12, 2002



**Tuan H. Nguyen**  
**Primary Examiner**